6) structures containing more complicated IC's can be created because the invention allows for increased I/O pin count.

7) more complicated IC's can be created without the need for a significant increase in re-distribution of package I/O connections.

8) power buses and clock distribution networks are easier to integrate within the design of IC's.

9) future system-on-chip designs will benefit from the present invention since it allows ready and cost effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

10) form the basis for a computer based routing tool that automatically routes interconnections that exceed a pre-determined length in accordance with the type of interconnection that needs to be established.

11) provide a means to standardize BGA packaging.

12) be applicable to both solder bumps and wirebonding for making further circuit interconnects.

13) provide a means for BGA device solder bump fan-out thereby facilitating the packing and design of BGA devices.

14) provide a means for BGA device pad relocation thereby providing increased flexibility for the packing and design of BGA devices.

15) provide a means for common BGA device power, ground and signal lines thereby reducing the number of pins required to interconnect the BGA device with the surrounding circuits.
16) provide a means for more relaxed design rules in designing circuit vias by the application of sloped vias.
17) provide the means for extending a fine-wire interconnect scheme to a wide-wire interconnect scheme without the need to apply a passivation layer over the surface of the fine-wire structure.

Although the preferred embodiment of the present invention has been illustrated, and that form has been described in detail, it will be readily understood by those skilled in the art that various modifications may be made therein without departing from the spirit of the invention or from the scope of the appended claims.